REMARKS

Claims 1-6 are pending herein.

I. The obviousness rejections of claims 1 and 3-5 based on Harada (US 2002/0195643), as noted on page 2 of the Office Action.

The USPTO respectfully rejects claims 1 and 3-5 under 35 U.S.C. § 103(a) as being unpatentable over Harada. Claims 1, 4, and 5 are independent claims.

A. Harada does not teach or suggest that the interface layer comprises an oxide of silicon, as claimed in claim 1, 4, and 5.

Claim 1 claims in relevant part:

> "**the interface layer comprises an oxide of silicon** formed so as to be mutually diffused with the silicon substrate, and a high dielectric constant metal element." (**emphasis added**)

Claims 4 and 5 claim similar limitations. No new matter is added by the amendments. Support for the amendments is found on page 5, line 29 though page 6, line 1 and page 6, lines 23-27. Regarding these limitations, it is respectfully not seen where Harada teaches or suggests the specifically claimed interface layer quoted above.

For example, the USPTO respectfully argues on page 2 of the Office Action that layer 11b of Harada is the specifically claimed interface layer. However, it is respectfully important to note that **Harada does not teach or suggest that layer 11b comprises an oxide of silicon**, as claimed in claims 1, 4, and 5. Instead, Harada respectfully teaches that layer 11b comprises a "silicon oxynitride film," which is different from the specifically claimed "oxide of silicon" claimed in claims 1, 4, and 5.

In contrast, present Figure 1 illustrates one possible embodiment of the claimed interface layer quoted above. As seen in Figure 1, a semiconductor device may include an interface layer 5. As explained on page 5, line 29, through page 6, line 1 of the present specification, **interface layer 5 may include $HfSiO_4$ (hafnium silicate),** which comprises an

oxide of silicon as claimed in claims 1, 4, and 5. As further explained on page 6, lines 23-27, **the interface layer 5 may also comprise $ZrSiO_4$ or $TiSiO_4$**, which also comprise an oxide of silicon, as claimed in claims 1, 4, and 5.

The distinction noted above is important and non-trivial because it results in significant advantages over conventional devices and methods. For example, it is respectfully important to note that **the presence of nitrogen at an interface of silicon in a semiconductor device deteriorates the characteristics of the semiconductor device** (for example, see pages 1-2 of the present specification, which describe this problem).

Thus, as noted above, the layer 11b in Harada comprises a silicon oxynitride film, and thus the nitrogen present in the oxynitride would deteriorate the characteristics of the semiconductor device. In contrast, **in claims 1, 4, and 5, the specifically claimed interface layer comprises an oxide of silicon, and not an oxynitride, and thus it is possible to form a high-quality semiconductor device.**

Thus, it is respectfully asserted that Harada does not teach or suggest all of the limitations of claims 1, 4, and 5. Therefore, it is respectfully asserted that claims 1, 4, and 5 are not obvious over Harada.

B. Further explanation.

Applicants respectfully note the following further explanation regarding independent claims 1, 4, and 5.

It is respectfully noted that the specifically claimed interface layer of claims 1, 4, and 5 does not contain nitrogen and contains a high dielectric constant metal element (high-k metal element), and an oxide of silicon. Therefore, the transistor property of the semiconductor device does not deteriorate due to the presence of nitrogen.

Additionally, the diffusion suppressing layer, which is excellent in electric insulation, is formed between the interface layer and the high dielectric constant insulating film (high-k film). Therefore, the thickness of the interface layer is not increased by heat treatment in the process of producing the transistor (see also page 2 of the present specification).

Also, the constitutional material of the high-k film is suppressed from being diffused toward the silicon substrate, and oxygen contained in the high-k film is suppressed from being diffused toward the interface layer. As a result, it is possible to prevent effectively the high dielectric constant (high-k) property which the high-k film originally has from being damaged.

Thus, by the synergetic effect of the above-mentioned advantages, a gate insulating film having a large dielectric constant can be formed, thereby obtaining a high-quality semiconductor device.

II. The obviousness rejections of claims 2 and 6 based on Harada in view of Bai (US 2001/0013629), as noted on page 4 of the Office Action.

The USPTO respectfully rejects claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Harada in view of Bai.

As noted above, it is respectfully asserted that independent claim 1 is allowable, and it is further respectfully asserted that Bai does not overcome the deficiencies noted above in section I regarding independent claim 1. Therefore, it is further respectfully asserted that dependent claims 2 and 6 are also allowable.

III. Conclusion.

Reconsideration and allowance of all of the claims is respectfully requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Please contact the undersigned for any reason. Applicants seek to cooperate with the Examiner including via telephone if convenient for the Examiner.

Respectfully submitted,

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